REMARKS

Claims 12-16 are pending in the Application. Claim 12 has been amended. Claims 17-18 have been cancelled herein. Claims 1-11 and 19-27 were previously cancelled in response to two different restriction requirements. The application has been carefully reviewed in light of the Office Action mailed on October 24, 2003. Reconsideration of all outstanding rejections in light of the foregoing amendments and following remarks is respectfully requested.

Amended claim 12 has been amended to include the limitations of claim 18. Amended claim 12 recites, *inter alia*, a "semiconductor package comprising a substrate having an upper surface, a lower surface, and an edge region disposed between said upper and lower surfaces, said edge including a first cut portion and a second broken portion comprising a sheared portion."

Cancelled claim 18 depended from claim 12 and was rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamaoka, *et al.*, (JP 10-064854)(hereinafter Yamaoka) and further in view of Itai, *et al.* (U.S. Patent No. 5,838,069)(hereinafter Itai).

The Office Action states on page 5 that Yamaoka did not disclose an edge region disposed between an upper and lower surface, the edge including a broken portion comprising a sheared portion. The Office Action continues stating that Itai disclosed the missing broken portion comprising a sheared portion citing Itai at COL. 2, lines 20-24 and 41-48. However, an examination of the cited sections of Itai reveals that the cited sections of Itai refer to a shearing force caused by differences in thermal expansion coefficients between an integrated circuit chip and a substrate the chip is mounted upon as well as thermal expansion differences between the substrate and a motherboard. (Itai, COL. 1, lines 55-61). The shearing force in Itai is developed in particular between chip and substrate connections, i.e. pads or terminals, which are on separate sections of the substrate (COL. 2, lines 1-5 referring to shearing force between two pads or terminals; COL. 2,

lines 21-24 referring to "joint portions" or terminal connections)

Moreover, there is no disclosure in Itai of, *inter alia*, "... an edge region disposed between said upper and lower surfaces, said edge including ... a second broken portion comprising a sheared portion." First, the Office Action cites sections of Itai which reference a "shearing force" between an a upper surface of Itai's substrate and an IC chip thereon (COL. 2, lines 21-24 and 41-44), not "an edge region disposed between said upper and lower surfaces ..." as in amended claim 12. (emphasis added) Secondly, Itai does not disclose, *inter alia*, a "substrate having ... a sheared portion". Rather, the only sheared portions disclosed in the sections of Itai cited by the Office Action are the sheared terminals or pin connections between an integrated circuit and a substrate after shearing of the terminals occurs due to unwanted thermal expansion. Accordingly, claim 12, as amended, is allowable over Yamoaka and Itai.

Claims 13-16 depend from amended claim 12, thus are allowable along with claim 12, and for other reasons.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

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Respectfully submitted,

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